Bulk Biased RF Energy Harvesting Dedicated to 900MHz/2.4GHz ISM Bands

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***Abstract*— The Radiofrequency (RF) energy harvesting is a widespread technique to extend the lifetime of devices in low power applications such as Wireless Sensor Networks (WSNs). Among the key building blocks featuring the RF harvester, the rectifier converts the incident AC signal into a DC output voltage. This paper presents the comparison between a multi-stage traditional CMOS voltage multiplier and a multi-stage voltage multiplier using bulk biasing to overcome the threshold voltage drop. The two rectifiers operate at 900MHz and 2.4GHz ISM bands and are prototyped using a standard CMOS 130nm process. The bulk-biased rectifier achieves a significant increase in power efficiency and low voltage-drop. Considering a case of study for supplying a load of 3.6 µW, the overall power efficiency reaches 48%, which is an improvement of 17% compared with the traditional circuit.**

Keywords—Harvesting; rectifiers; bulk biasing technique; low power devices; power efficiency

I. INTRODUCTION

Nowadays there is a growing demand for large-scale applications as RFID circuits and sensor-based wireless networks. Within such context the need for green communication strategies and inexpensive solutions is of great importance. One approach is to set up a network comprising self-powered nodes, i.e., nodes that can harvest ambient energy from a variety of natural and man-made sources for sustained network operations [1]. This yields a significant reduction in the maintenance costs associated with periodically replacing batteries or providing extended battery life by implementing highly efficient power management capabilities, or to wake up remote sensors in sleep mode.

Since input RF signal voltage available for many power harvesting applications at far-end position is quite small, it is critical to have a high efficient rectifier. In order to obtain high voltage gain and power conversion efficiency, Schottky diodes are considered as an attractive candidate to perform the charge transfer task due to their low forward voltage drop, low substrate losses and fast switching speed [2]. However, their integration is complex and expensive. Thus, they are not supported by standard CMOS technologies which focuses on low-cost applications throughout a high level of integration.

Usually CMOS implementation is achieved by utilizing diode-connected MOS transistors in Dickson charge pump. Power efficiency of the rectifier is affected by instantaneous threshold voltage drop across the switches [3-5]. In [6], a comparator is used to control NMOS transistors to operate as a switch in order to reduce the dropout voltage, which however, can only be applied in active or semi passive sensors. High efficiency for low input voltage is achieved in [7] by using floating gate transistors as rectifying diodes. However, the lower transistor threshold voltage obtained by floating-gate rectifiers increases input capacitance and layout area. Furthermore general purpose CMOS processes are not furnished with two Polysilicon layers, making floating gates unfeasible.

In many power harvesting applications, such as WSNs and RFID, the cost prevails over the performances. Within a context of efficient trade-off between circuit performances and overall node cost, the rectifiers reported in this work are developed in a 130nm standard CMOS process. Hence, an architecture using bulk-biasing technique to overcome the threshold voltage drop is proposed and detailed in the following sections in order to obtain better performances in the scenario of long range wireless power transfer (WPT).

The paper is organized as follow. Section II introduces the rectifier architectures with the description of both voltage multiplier architectures, using bulk biasing and traditional technique. Section III presents schematic and post-layout simulation (PLS) results from all structures as well as a comparison between them followed by the conclusions in Section IV.

II. OVERVIEW OF THE RECTIFIERS

A. Traditional Voltage Multiplier

The schematic of a traditional half-wave rectifier is illustrated in Fig. 1. To describe its operation , a single stage structure is first analyzed.

During the negative half cycle of the RF signal, when $V_{DrainM1} > V_{IN} + V_{Th}$, the transistor M_1 turns on while transistor M_2 turns off as $V_{CG} < V_{OUT}$. The charge then starts to be transferred to capacitor C_{IN}. The DC voltage at V_{CG} node is therefore $V_{IN} + V_{DrainM1} - V_{Th}$.

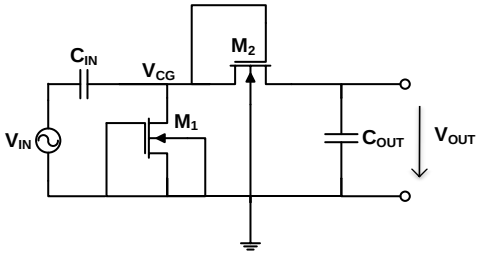


Fig. 1. One-stage traditional voltage multiplier architecture.

When the input changes to the positive half cycle, the transistor M_1 turns off while transistor M_2 turns on and the charge is transferred from capacitor C_{IN} to capacitor C_{OUT}. The capacitor C_{IN} is the coupling capacitor, which is responsible for the electric charge transfer. At the end of the cycle, the energy is stored in C_{OUT}, storage capacitor. The final available output voltage V_{OUT} is expressed as:

$$V_{OUT} = 2 \cdot (V_{IN} - V_{Th}) \quad (1)$$

where V_{IN} is the input RF signal amplitude and V_{Th} the threshold voltage of MOS transistor.

The maximum voltage that can be achieved in a single stage traditional voltage multiplier is twice the RF amplitude voltage minus twice the threshold voltage of the diode-connected MOS.

To increase the rectified voltage, several cells of the basic multiplier can be cascaded as proposed in Fig. 2.

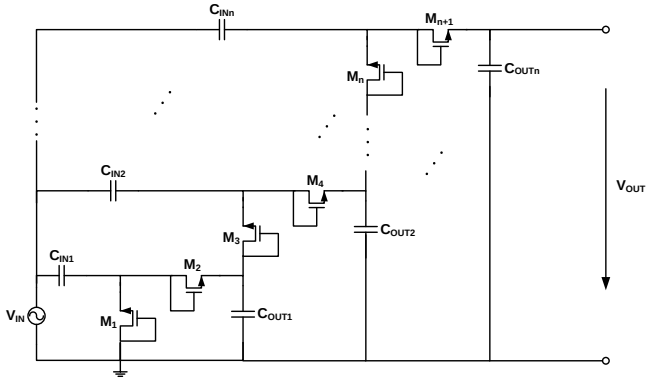


Fig. 2. N-stage traditional voltage multiplier architecture.

In this case, a higher output voltage is obtained through the accumulation of stored charge transferred from the output of one stage to the input of the following. After cascading several voltage multipliers, the generated voltage at C_{OUTn} is multiplied by the number of used stages:

$$V_{OUT} = 2 \cdot n \cdot (V_{IN} - V_{Th}) \quad (2)$$

Equation (2) figures out that the threshold voltage has a significant effect on the output voltage and needs to be minimized to improve the rectifying efficiency. Moreover, increasing the number of stages practically generates a power dissipation growth and, consequently, a power conversion efficiency drop in low power applications.

B. Bulk-biased Voltage Multiplier

Threshold voltage is a process dependent parameter which is linked to the oxide properties. Some standard CMOS processes offer low and medium threshold devices which could be used to perform low-threshold designs. However, their availability is not yet generalized, and such devices are subject to significant leakage due to higher channel doping leading to excessive power consumption and reliability problems. Thus, low-threshold devices are generally not good candidates to be integrated in the main flow of current towards the load.

According to (2), one approach to improve the rectifier performance is to decrease the transistors threshold voltage drop. It is possible by biasing the body or bulk of the transistors, this condition is reached ensuring faster turn on during the conduction phase while reducing the leakage current during the non-conducting phase. The transistor MOS threshold voltage is expressed as:

$$V_{Th} = V_{Th0} + \gamma\left(\sqrt{2|\varphi_S| + V_{SB}} - \sqrt{2|\varphi_S|}\right) \quad (3)$$

where V_{Th0} is the threshold voltage of the long channel device at zero substrate bias, γ the body bias coefficient and φ_S the surface potential; all these parameters are related to the used technology.

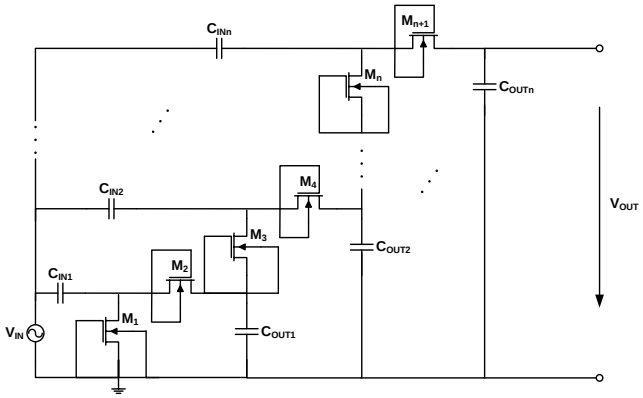


Fig. 3. N-stage gate bulk-biased voltage multiplier architecture.

Analyzing the N-stage bulk-biased voltage multiplier presented in Fig. 3, we can notice that the transistors operate either in saturation or in sub-threshold mode. During the conduction phase, the sources of transistors M_1 and M_2 are respectively connected to V_{CG} and V_{OUT} nodes. In this case, their gates are tied to their drains, making a positive V_{GS} required to turn on the transistors. As stated in (3), the only parameter which can be tuned is V_{SB}. Then, a simple way to improve V_{Th} without adding more complex circuits is to connect the bulk to the drain, since the drain voltage is always higher than the source one in this phase.

Considering the non-conduction phase, the transistors change their polarity. Now the drain of M_1 and the source of M_2 are connected to V_{CG} node and their gates are tied to their sources, ensuring sub-threshold operation mode. During this cycle, PN junctions must be taken into account. Actually, bulk-biasing the transistors in this operation mode could turn on parasitic diodes, mainly if input voltage exceeds 250mV, where forward bias of PN junction begins to degrade the rectifier performances for low-power applications.

Usually to power supply a load of 3.6µW at 1.2V, the input voltage amplitude required must be higher than 250mV. Therefore, it is better to improve the body-effect during turn on phase only. Finally, the bulk-biasing configuration chosen here is to connect the bulk at the same node as the gate, where an improvement is provided during turn on phase, while avoiding losses during turn off mode.

C. DC Bulk-biased Voltage Multiplier

The topology proposed in Fig. 4 uses the same body effect technique described in previous architecture to improve voltage multiplier performances, in addition to ensure a stable operation without degrading power conversion efficiency due to parasitic devices in bulk isolation.

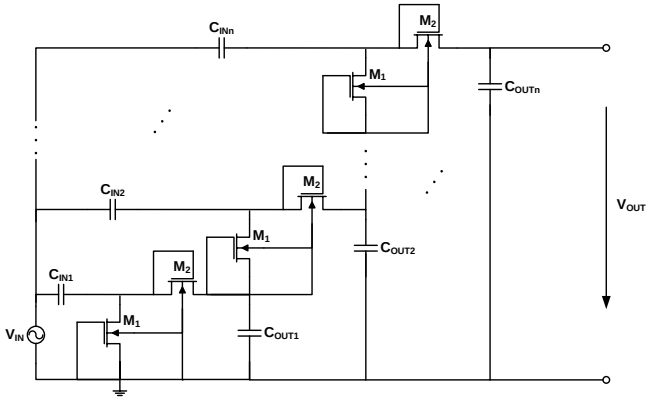


Fig. 4. N-stage DC bulk-biased voltage multiplier architecture.

To power supply transistors bulk with different voltages than ground, their substrate must be isolated. To establish a good operation mode, the isolation must be supplied with the highest voltage in the circuit. As the different DC power supplies existing in such devices are converted by themselves, it is difficult to avoid higher peak voltages inside the circuit than the provided DC voltages in output stages.

All transistors used into these rectifying circuits are NMOS, so an N type well insulation is required to surround them, which includes PN parasitic diodes into the circuit. Connecting the anode side into an AC signal is not a good option, since that could start their conduction, increasing the losses.

To guarantee that the N-well insertion does not increase the power dissipation, the bulk-biasing strategy chosen in this topology consists in connecting all transistor's bulks with a DC voltage, which improves the power conversion on turn on mode, but not as good as dynamic bulk-biasing as detailed in II.b, and at the same time ensures all probably parasitic devices to stay turned off. Among several DC nodes, the transistor body bias in this architecture uses the DC voltage provided by previous stage as shown in Fig. 4.

III. SIMULATION RESULTS

Both the conventional and proposed bulk-biased voltage multipliers have been designed and laid out in a 130nm CMOS technology. The transistor sizes are optimized to drive a 400 kΩ/1.2V load, representing an output power of 3.6µW. Under these conditions, the number of stages for cascaded traditional voltage multiplier and cascaded bulk-biased voltage multiplier are 3.

These circuits are designed to operate into the 900 MHz and 2.4 GHz ISM bands. The power sensitivity P_{IN}, efficiency η and input voltage of the three circuits are compared in the following parts.

TABLE I. PLS RESULTS FOR TRADITIONAL AND BOTH BULK-BIASED RECTIFIERS IN 900 MHZ AND 2.4 GHZ FOR A FIXED OUTPUT POWER.

	Traditional		**Bulk-biased**		**DC Bulk-biased**	
	0.9GHz	***2.4GHz***	***0.9GHz***	***2.4 GHz***	***0.9GHz***	***2.4GHz***
V_{OUT} [V]	1.2	1.2	1.2	1.2	1.2	1.2
V_{IN} [mV]	505	505	420	420	450	450
P_{IN} [dBm]	-20.4	-20	-21.3	-20.7	-20.9	-20.2
η [%]	41	34	48	41.5	44	37

Table I shows rectifier performances for an output power fixed to 3.6 µW under a 1.2 V voltage supply. Under these conditions, the bulk-biased voltage multiplier presents an increase of about 17% of power transfer efficiency, when compared with the conventional structure. On the other hand, the DC bulk-biased topology presents an improvement of 8% when also comparing with the conventional topology.

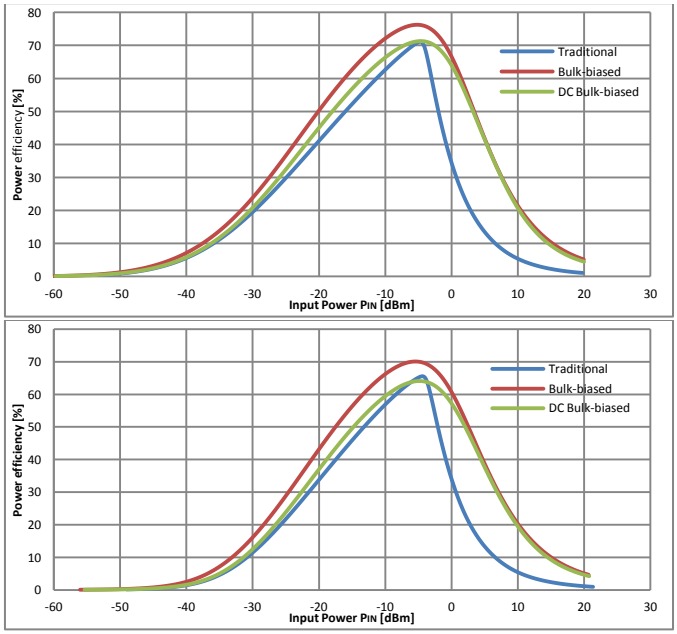


Fig. 5. Power efficiency as a function of input power for 0.9 (a) and 2.4 GHz (b).

The power efficiency evaluation as a function of input power is presented in Fig. 5 and the output DC voltage, V_{OUT}, as a function of the input power, P_{IN}, is reported in Fig. 6 for 900MHz and 2.4GHz. It is depicted that both bulk-biased voltage multipliers provides a higher output power as a function of input power with respect to traditional rectifier, which confirms an improvement in sensitivity, allowing their operation in lower power conditions. Furthermore, considering an output power of 3.6 µW, the bulk-biased technique exhibits an input power, P_{IN}, of -21.3 dBm to drive a 400 kΩ load at 1.2 V, whereas the traditional circuit requires -20.4 dBm, which is an improvement of about 1 dB in sensitivity.

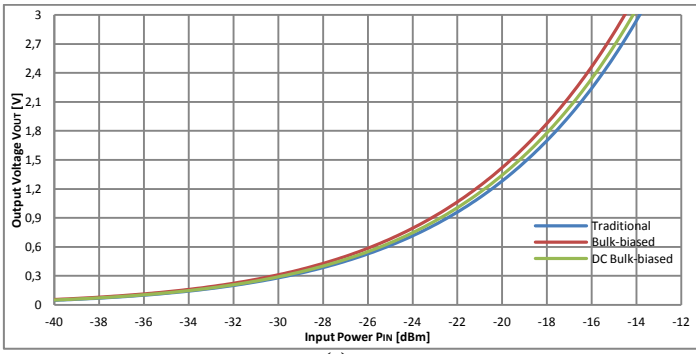
It should be noted that only information about input RF power is not necessarily enough to evaluate the performances

of a rectifier, except if it comes with the information about the input voltage level. The peak voltage available at the input, under perfect power matching condition, is given by [8]:

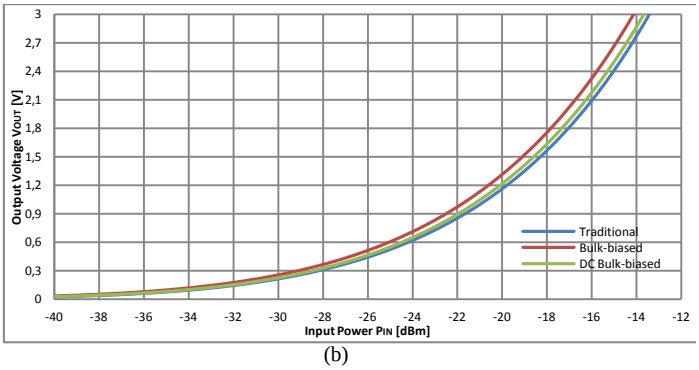
$$V_{IN} = \sqrt{\frac{P_{IN}}{R_A}} \frac{1}{\omega C} \quad (4)$$

where P_{IN} is the available power at the antenna terminals, R_A the antenna equivalent resistance, ω the resonance frequency of the antenna impedance and C the chip equivalent input capacitance. To enhance the input voltage seen by the chip, R_A has to be minimized; however, the minimum antenna impedance is dictated by geometrical constraints and maximum efficiency. So, at a large distance from the RF source, where the incoming rectifier power is small, a little input voltage is received, which impairs the proper operation of the differential rectifier.

Thus, to ensure a long range of operation, a small turn-on voltage is as important as a small power-up threshold. Table I shows the input voltage achieved through both bulk-biased architectures and traditional technique under desired conditions. It can be noted that the bulk-biased voltage multipliers require lower input voltage compared with a conventional one, confirming the theory.



(a)

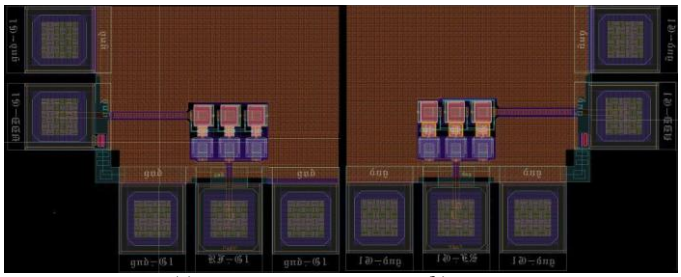


(b)

Fig. 6. Output voltage as a function of input power for 0.9 (a) and 2.4GHz (b).

According to Fig. 5 (a) and (b), the rectified power at 900MHz is higher than at 2.4GHz as expected. This difference comes from parasitic losses of MOS devices which increase with their frequency.

Fig. 7 depicts the 3 stage traditional and bulk biased rectifier layouts. All voltage multiplier circuits silicon area are 322x410 μm² with PADs included. Their core areas are around 80x100 μm².



(a) (b)

Fig. 7. Traditional (a) and bulk biased (b) voltage multiplier layouts.

IV. Conclusions

Two different multi stage voltage multipliers using bulk biasing to overcome the threshold voltage drop and a conventional architecture are reported in this work. The bulk-biasing topology significantly improves the power efficiency compared to a traditional one.

As a case of study, two circuits were implemented in a 130nm standard CMOS technology and optimized to drive a typical 400kΩ/1.2 V load at 900 MHz and 2.4 GHz. Under this conditions, the 3-stage voltage multiplier using bulk-biasing technique exhibits better power conversion efficiency over traditional circuit, 48% at -21.3dBm by bulk-biasing voltage multiplier and 44% at -20.9dBm by DC bulk-biased architecture, whereas the conventional voltage multiplier achieves 41% at -20.4dBm. This result is a significant improvement in both power conversion and sensitivity. This higher sensitivity of the multi stage bulk-biased voltage multiplier architecture makes it more suited for a long range wireless power transfer –i.e. over several meters- as well as opportunistic RF energy scavenging.

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