A HIGH THROUGHPUT MULTIPLIERLESS LOW POWER 8X8 2-D DCT IP FOR PORTABLE MULTIMEDIA APPLICATIONS

Vinícius dos S. Livramento, Bruno G. Moraes, Brunno A. Machado, José Luís Güntzel
{vini, brunogm, guntzel}@inf.ufsc.br
brunno@das.ufsc.br
Federal University of Santa Catarina
Department of Informatics and Statistics

ABSTRACT

This paper presents a high throughput multiplierless low power IP core for the 8x8 2-D DCT. It relies on a fast and precise implementation of the LLM algorithm. The IP architecture explores the separability property, using a single 1-D DCT, implemented as a combinational block, an 8x8 register file and a control unit. The 1-D DCT block can operate at 5 MHz thus achieving a throughput of 19 Mpixels/s (VGA@30fps), as required by a typical contemporary portable multimedia application. Synthesis results for the XFAB 350nm CMOS technology estimate total power as 7.65mW and core chip area as 3.20mm$^2$. In order to allow the comparison with related works, we used the mJ/Mpixels metric. Under such metric, the designed IP is at least twice as efficient as other 2-D DCT architectures presented in related works.

1. INTRODUCTION

Multimedia applications are present in most of contemporary portable electronic devices, such as smartphones and digital cameras. Such kind of applications demands high computational performance that, by its turn, results in significant power consumption, shortening battery lifetime. Image and video applications are heavily based on the Discrete Cosine Transform (DCT) [1], which is widely used in JPEG [2] and MPEG2 [3] multimedia coding systems. The high computational cost of the DCT and the demanded energy efficiency for battery-operated portable devices motivate the investigation of low-power DCT hardware architectures.

A contemporary smartphone has a built-in camera with up to 8 Mpixles of resolution, being capable to process a color still picture in YCbCr [4] with 4:2:2 subsampling format. Under such format, a single picture is represented by luma components (Y) and chroma components (Cb, Cr), each one organized as 8x8 8-bit pixel matrices. In the present paper the throughput is defined in Mega pixels per second and includes color information from the image. Therefore, for the smartphone mentioned above, which may be considered as a potential target application, the required throughput for a still picture is 16 Mpixles/s.

For the same target application, the throughput for the VGA@30fps video format is 18.432 Mpixles/s. Assuming this throughput, Table 1 shows other achievable video formats.

<table>
<thead>
<tr>
<th>Frame Rate</th>
<th>VGA (640x480)</th>
<th>30 fps</th>
</tr>
</thead>
<tbody>
<tr>
<td>480x360</td>
<td>53 fps</td>
<td></td>
</tr>
<tr>
<td>CIF (352x288)</td>
<td>90 fps</td>
<td></td>
</tr>
<tr>
<td>QVGA (320x240)</td>
<td>120 fps</td>
<td></td>
</tr>
</tbody>
</table>

Many algorithmic approaches for the 8x8 2-D DCT can be found in the literature. The two most used solutions are the direct 2-D transform and the row/column decomposition, which computes the 2-D DCT as a sequence of two 1-D DCT computations and a transposition. Such an approximation is possible thanks to the so-called separability property of the 2-D DCT. This work adopts the latter solution since it leads to lower computational complexity, which may be explored to minimize the cost of the hardware. In addition, the lower computational complexity leaves room for exploring the tradeoff between performance and power consumption, by low power architectural exploration, possibly applying low power techniques such as Multi-Vdd and Multi-Vt [14].

A few fast 1-D DCT algorithms, such as the LLM [5] and the AAN [6], use butterflies processing and even/odd decomposition to reduce redundant computation.

Among the architectural solutions found in the literature, the 2-D DCT architectures proposed by Hsia [7], by Kinane [8] and by Agostini [9] are the ones that are nearest to the features presented by the architecture of this work. Therefore, they were selected to establish the comparisons.

The 2-D DCT proposed by Hsia [7] uses a low cost transposeless 1-D scheme with a particular scheduling order whose objective is to eliminate the need for a transpose operation between the two 1-D blocks. This is accomplished by using an off-chip memory. Kinane's solution [8] uses the 1-D scheme with a transpose memory using even/odd decomposition and a distributed arithmetic adder summation tree. This architecture also presents a shape adaptive structure with the DCT. The architecture presented by Agostini [9] is composed of two 1-D DCT blocks and a transpose buffer in-between. The multiplications are decomposed into shift-add operations.

This work is partially supported by CNPq Brazilian Agency, through the Brazil IP project.
Our approach is based on Massimino’s fast and precise LLM algorithm [10]. It performs two 1-D DCT computations that operate over rows and columns, respectively. In our implementation, a few particular architectural decisions were taken so as to minimize power consumption.

This paper is organized as follows. The 2-D DCT algorithm is presented in Section 2. The implemented architecture is detailed in Section 3. Synthesis results are shown in Section 4. Section 5 draws some conclusions.

2. THE CHOSEN 2-D DCT ALGORITHM

Table 2 shows the IEEE 1180 conformance [13] results for Massimino’s 2-D DCT algorithm, reported by the own author. In this table, PE, PME, PMSE, OME and OMSE stand for peak error, peak mean error, peak mean square error, overall mean error, and overall mean square error, respectively. The reported conformance values indicate the high precision, which is one of the main reasons for choosing this algorithm for a hardware realization.

Considering 8x8 matrices, as used in the architecture presented in section 3, the complexity of Massimino’s algorithm is $O(N^2 \ln N)$, where N is the DCT size.

Massimino’s algorithm computes the 2-D DCT by using the row/column decomposition, that is, by two subsequent 1-D DCT computations and a transposition. Each 1-D computation is divided in two main parts: the first one realizes the initial butterflies, whereas the second one corresponds to the even/odd decomposition with four rotations, totaling twelve multiplications. The rotations are decomposed using the following equations:

$$\text{tmp} = (x+y) \cdot \cos t \quad \text{(1)}$$
$$x' = \text{tmp} + y \cdot (\sin t - \cos t) \quad \text{(2)}$$
$$y' = \text{tmp} - x \cdot (\sin t + \cos t) \quad \text{(3)}$$

Also, the rotations were further reduced by common sub-terms factorization using the following trigonometric identity for the special case $b=\pi/16$:

$$\cos(a)\cos(b) - \sin(a)\sin(b) = \cos(a+b) \quad \text{(4)}$$

Each rotation has three multiplications, totaling twelve multiplications for each 1-D computation. The cosine constants used in the multiplications are integers. That is another reason for choosing Massimino’s algorithm. After all simplifications are done, the algorithm ends up with four rotations, some additions and a row/column decomposition. Those operations are quite simple and thus appropriate for direct hardware implementations.

3. 2-D DCT PROPOSED ARCHITECTURE

Originally, the algorithm performs the operations using nineteen-bit width constants. However, in order to reduce the amount of resources needed to implement it directly on hardware we recalculated the values of the constants in such a way that each constant is represented with fourteen bits. The new version of the algorithm incorporating such modifications was also submitted to the IEEE 1180 conformance tests. The results showed an error smaller than 0.01% for the OME and an error of 20% for OMSE with respect to the original version, whereas PME and PMSE did not change. Such results indicate a negligible loss of precision, despite the significant reduction in the resources achieved.

Due to the high cost of hardware multipliers and considering that only multiplications by constants are needed, the proposed architecture adopts only shift-add operations (as does Agostini’s [9]). This hardware optimization does not imply in any precision loss, since the constants used in Massimino’s algorithm are integers.

The design of the 2-D DCT architecture aimed at a throughput of 19 Mpixels/s, considering that a contemporary portable multimedia device needs 18,432 Mpixels/s to process video in VGA@30fps with 4:2:2 format and 16 Mpixels/s to process an 8 Mpixel still image with 4:2:2 format. The design also takes advantage of the separability property by using a single 1-D DCT block. A transpose buffer, built up from a register file and a control unit (FSM), supplies the 1-D DCT block with the 14-bit data matrix. The IP core interface consists of eight 8-bit data inputs, eight 12-bit data outputs, and control signals to perform the handshake according to the AMB-AXI protocol [13].

As a first step, the TBUFFER receives data from the data inputs, storing them in the registers in a row order. Then it feeds the 1-D DCT block with data stored in the registers following the row order and commands the storage of the results back to the registers, also in row order. In a third step, the TBUFFER feeds the 1-D DCT block with data stored in the registers following the

<table>
<thead>
<tr>
<th>Input pixel range</th>
<th>PE $(&lt;1)$</th>
<th>PME $(&lt;0.015)$</th>
<th>PMSE $(&lt;0.06)$</th>
<th>OME $(&lt;0.0015)$</th>
<th>OMSE $(&lt;0.02)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-256 ~ 255</td>
<td>1.0000</td>
<td>0.0191</td>
<td>0.0340</td>
<td>-0.0033</td>
<td>0.0200</td>
</tr>
</tbody>
</table>
column order and commands the storage of the results back to the registers, also in column order. Finally, the resulting matrix is released by a row order read of the registers.

The parallelism provided by the architecture allows an 8x8 matrix to be read in 8 clock cycles. At the same time the data is read in it is processed in the 1-D DCT block. At the end of each cycle the results from the 1-D DCT are written back to the register file. Therefore, the row order 1-D DCT computation is accomplished in 8 clock cycles. More eight cycles are needed to perform the column order 1-D DCT computation. Finally, the whole resulting matrix is delivered in row order in another eight cycles. A straightforward optimization relies on not waiting until the whole resulting matrix to be delivered in order to begin the processing of a new matrix. At the same time the resulting matrix is being released, a new matrix begin to be processed, improving the throughput.

Figure 2 shows the IP timing diagram. Note that the latency is twenty-four cycles whereas the time to deliver a new matrix is seventeen cycles, considering steady operation. Such processing time leads to an estimated throughput of 19 Mpixels/s when operating at 5MHz.

The 1-D DCT block was designed as a fully combinational block. Such design decision was motivated by the following reasons:

- The level of parallelism used in the architecture makes possible to compute the 1-D DCT of a whole row or column within a single clock cycle, thus avoiding the cost and power consumption of a pipeline processing.
- The control unit is simple.
- Lower clock frequency as compared to a pipeline version leading to lower switching activity.
- The combinational 1-D DCT leads to a clock slack that is longer than that of a pipelined structure, opening the possibility to apply advanced low power techniques such Multi-Vdd and Multi-Vt [14].
This paper presented an 8x8 2-D DCT architecture for high throughput low power IP core. High throughput is achieved by using an 8-element parallelism and a combinational 1-D DCT. The low power is achieved by avoiding the expensive pipeline structure, using a simple architecture built upon a 1-D DCT combinational block and a register file to implement the transposition. Such features lead to low clock frequency, resulting in lower switching activity.

The proposed architecture shows to be at least 2.4 times more efficient in terms of the considered mJ/Mpixels metric as compared to 2-D DCT architectures presented in related works. The reported critical path slack suggests a broader space to explore for further power improvements.

6. REFERENCES


5. CONCLUSION

### Table III. Synthesis results

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Process [nm]</th>
<th>Voltage [V]</th>
<th>P (Total) [mW]</th>
<th>mW/ (Mpixels/s)</th>
<th>Area [mm²]</th>
<th>Latency [Clk cycles]</th>
<th>Speed [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agostini*</td>
<td>350</td>
<td>3.3</td>
<td>41.67</td>
<td>2.19</td>
<td>2.34</td>
<td>163</td>
<td>19</td>
</tr>
<tr>
<td>Hsia [3]</td>
<td>350</td>
<td>3.3</td>
<td>15</td>
<td>0.96</td>
<td>4.00</td>
<td>22</td>
<td>60</td>
</tr>
<tr>
<td>Kinane [4]</td>
<td>350</td>
<td>3.3</td>
<td>15</td>
<td>3</td>
<td>n/a</td>
<td>142</td>
<td>n/a</td>
</tr>
<tr>
<td>Proposed</td>
<td>350</td>
<td>3.3</td>
<td>7.65</td>
<td>0.40</td>
<td>3.20</td>
<td>24</td>
<td>5</td>
</tr>
</tbody>
</table>

* Our synthesis results.